A1 cont.

19. (New) A method in accordance with claim 1 wherein said step of providing an isolation structure comprises providing an isolation structure including a CMOS well.

20. (New) A method in accordance with claim 9 further comprising the step of forming a contact layer of said first conductivity type overlying said first implant.

21. (New) A method in accordance with claim 9 wherein said first conductivity type and said second conductivity type are the same.

22. (New) A method in accordance with claim 9 wherein said step of providing an isolation structure comprises providing an isolation structure including a CMOS well.

23. (New) A semiconductor structure in accordance with claim 12 further comprising a contact layer of said first conductivity type overlying said first implant.

24. (New) A semiconductor structure in accordance with claim 12 wherein said first conductivity type and said second conductivity type are the same.

25. (New) A semiconductor structure in accordance with claim 12 wherein said isolation structure comprises a CMOS well.

sub. C3

26. (New) A method of forming a varactor device on a semiconductor substrate, comprising the steps of:

providing a semiconductor substrate having a first conductivity type;

forming a first implant in at least a portion of said semiconductor substrate using a first implant energy, said first implant having a first peak dopant concentration and a second conductivity type, wherein said first implant extends into said semiconductor substrate a first distance;

forming a second implant in at least a portion of said semiconductor substrate using a second implant energy, said second implant having a second peak dopant concentration and said second conductivity type, wherein said second implant extends into said semiconductor substrate a second distance, wherein said second distance is greater than said first distance.

27. (New) A method in accordance with claim 26, further comprising the step of forming a contact layer of said first conductivity type overlying said first implant.

A1 cont.

28. (New) A method in accordance with claim 26 wherein said first conductivity type and said second conductivity type are the same.

29. (New) A method in accordance with claim 26, further comprising the step of annealing the device following the steps of forming said first implant and said second implant.

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30. (New) A method in accordance with claim 26, further comprising the step of selecting said first peak dopant concentration and first implant energy such that at least one of capacitance, leakage current, and tuning range of the varactor device is optimized.

31. (New) A method in accordance with claim 26, wherein said selecting step comprises determining an as-implanted dopant concentration profile for said first implant.

32. (New) A method in accordance with claim 31, wherein said step of determining an as-implanted dopant concentration profile is performed using secondary ion mass spectroscopy.

33. (New) A method in accordance with claim 26, further comprising the step of selecting said second peak dopant concentration and said second implant energy such that the base resistance of the varactor device is minimized.

34. (New) A method in accordance with claim 33, wherein said selecting step comprises determining an as-implanted dopant concentration profile for said second implant.

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35. (New) A method of forming a varactor device on a semiconductor substrate, comprising the steps of:

providing a semiconductor substrate having a first conductivity type;

forming a first implant in at least a portion of said semiconductor substrate using a first implant energy, said first implant having a first peak dopant concentration and a second conductivity type, wherein said first implant extends into said semiconductor substrate a first distance;

forming a second implant in at least a portion of said semiconductor substrate using a second implant energy, said second implant having a second peak dopant concentration and said second conductivity type,

A1 cont.

wherein said second distance is greater than said first distance, wherein said first peak dopant concentration and said first implant energy are selected such that at least one of capacitance, leakage current, and tuning range of the varactor device are optimized, and wherein said second peak dopant concentration and said second implant energy are selected with relation to said first peak dopant concentration and said first implant energy such that the base resistance of the varactor device is minimized.

36. (New) A method in accordance with claim 35 further comprising the step of forming a contact layer of said first conductivity type overlying said first implant.

37. (New) A method in accordance with claim 35 wherein said first conductivity type and said second conductivity type are the same.

38. (New) A semiconductor structure comprising a varactor device formed by the method of claim 26.

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39. (New) A semiconductor structure comprising a varactor device formed by the method of claim 35.

40. (New) A semiconductor structure having a varactor device formed therein, comprising:

a semiconductor substrate having a first conductivity type;

a first implant formed in at least a portion of said semiconductor substrate, said first implant having a first peak dopant concentration and a second conductivity type, wherein said first implant extends into said semiconductor substrate a first distance;

a second implant formed in at least a portion of said semiconductor substrate, said second implant having a second peak dopant concentration and said second conductivity type, wherein said second implant extends into said semiconductor substrate a second distance, wherein said second distance is greater than said first distance.

41. (New) A semiconductor structure in accordance with claim 40 wherein said first conductivity type is N-type.

42. (New) A semiconductor structure in accordance with claim 40 wherein said first conductivity type is P-type.

A1 conc.

43. (New) A semiconductor structure in accordance with claim 40 wherein said first conductivity type and said second conductivity type are the same.

44. (New) A semiconductor structure in accordance with claim 40 further comprising a contact layer formed overlying said first implant.

REMARKS

This preliminary amendment is being submitted to correct minor errors noted in the application as filed and to add claims to the application to better clarify the invention (44 total claims, 6 independent claims). No new matter is being added by this preliminary amendment. Support for newly added claims 17-44 is found, inter alia, in the originally-filed claims. Support for newly added claims 22 and 25 is found, *inter alia*, at page 4 lines 5-6 *et seq.* of the application. No office action has been received regarding this application since it was filed on June 9, 2000.

Our check for payment of the additional claims is attached hereto. Please charge any deficiency, or credit any overpayment, to Deposit Account No. 19-2814, **for which purpose a duplicate copy of this request is enclosed.**

Dated: 22 November 2000

Respectfully submitted,

By: _____
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